TDB-ACC-NO: NN8901114

DISCLOSURE TITLE: Self-Aligned Quasi-Semiconductor-On-Insulator CMOS Structure

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, January 1989, US

VOLUME NUMBER: 31

ISSUE NUMBER: 8

PAGE NUMBER: 114 - 115

PUBLICATION-DATE: January 1, 1989 (19890101)

CROSS REFERENCE: 0018-8689-31-8-114

DISCLOSURE TEXT:

- A technique is described whereby a self-aligned quasi-semiconductor- on-insulator (SOI)

CMOS structure is fabricated
so as to provide high performance, high density and high immunity to
latch up and soft errors. The self-aligned quasi SOI CMOS structure,
as shown in the figure, utilizes insulator layers buried underneath
the source and drain regions and self-aligned to gate channels,
source/drain, and isolation regions of the MOS device. The
self-alignment of the buried insulator layers is achieved in the same
way as that of the source and drain regions by the gate electrode and
the field isolation.

The key process step is to implant elemental species after the delineation of the gate electrode, which can later
be reacted with the substrate material, to form the buried insulator.

For example, oxygen or nitrogen can be implanted into the silicon
substrate to form silicon dioxide, or nitride, by subsequent heat
treatments. This structure is called a quasi-SOI, since only

source/drain diffusion regions are on the insulator. The resulting
product provides the following advantages:
$ Low capacitance in the diffusion areas.
- $ Firm substrate and well biases, eliminating problems
associated with the floating substrate in full SOI.
- $ Improved latch up immunity due to reduced emitter areas.
- $ Allows borderless contacts against diffusion/isolation
edges.
- $ The buried insulator layer can be used to control the
junction depth of the source/drain diffusions.
- $ There will be no junction leakage problems at the
diffusion-isolation edge caused by self-aligned
silicidation.
- $ The drains of complementary semiconductor devices in an
inverter circuit may be butted together on top of buried
insulator layers without an isolation

region in between.

- $ Minimum isolation dimensions, lithography limited, can be allowed since the short channel effect of the parasitic field device is essentially eliminated.
- $ Dense layout of circuits can be provided because of the improved isolation, latchup immunity, borderless contact and zero n+/p+ spacings. The fabrication process consists of the following four steps:

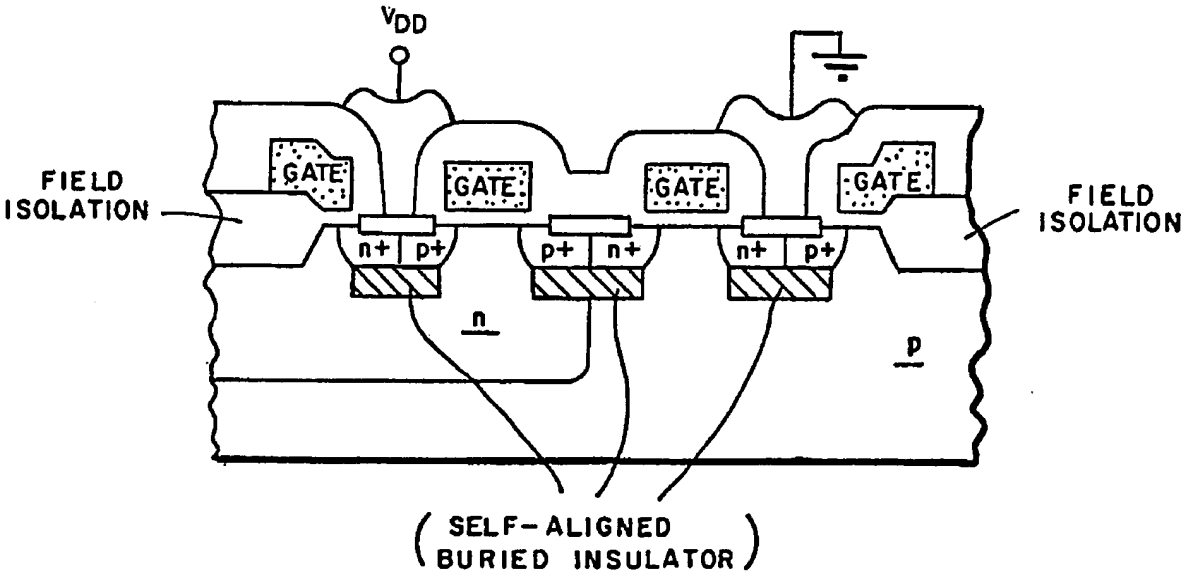
1) Thick insulator layers are deposited or grown on top of the gate layer and the whole stack is patterned and etched anistropically to delineate the gate electrode.

- These thick layers can be designed to provide the selectivity for the anistropic etching steps and to block the buried insulator implantation from the gate electrode and the channel region. Therefore, the buried insulator

is self-aligned to the gate and is also self-aligned to the field isolation region, if the field isolation layer is thicker than the projected range of the buried insulator implantation.

- 2) The buried insulator implantation is performed either before or after the source/drain implantation. The amount and energy of buried insulator implantation can be adjusted to give the optimum depth and thickness.
- Channel-stop doping is adjusted according to the depth of the buried insulator so as to provide adequate insulation among the active devices.
- 3) Rapid thermal anneal may be employed to synthesize the buried insulator without causing too much redistribution of dopants in the substrate and channel regions. Conventional thermal anneal can be used for

the synthesis of the
buried insulator if dopant redistribution is not a
problem.
- 4) Heavily doped regions for ohmic contacts can be formed by
implanting the same type of dopants as that of the
background next to the gate electrode, thereby producing
a non-FET structure.




The self-aligned quasi SOI CMOS structure, as shown in the figure, utilizes insulator layers buried underneath the source and drain regions and self-aligned to gate channels, source/drain, and isolation regions of the MOS device. The self-alignment of the buried insulator layers is achieved in the same way as that of the source and drain regions by the gate electrode and the field isolation. The key process step is to implant elemental species after the delineation of the gate electrode, which can later be reacted with the substrate material, to form the buried insulator. For example, oxygen or nitrogen can be implanted into the silicon substrate to form silicon dioxide, or nitride, by subsequent heat treatments. This structure is called a quasi-SOI, since only source/drain diffusion regions are on the insulator. The resulting product provides the following advantages:

- Low capacitance in the diffusion areas.
- Firm substrate and well biases, eliminating problems associated with the floating substrate in full SOI.

TDB-ACC-NO: NN84046022

DISCLOSURE TITLE: P and N Collar CMOS Technology

PUBLICATION-DATA: IBM Technical Disclosure Bulletin, April 1984, US

VOLUME NUMBER: 26

ISSUE NUMBER: 11

PAGE NUMBER: 6022 - 6023

PUBLICATION-DATE: April 1, 1984 (19840401)

CROSS REFERENCE: 0018-8689-26-11-6022

DISCLOSURE TEXT:

- This article relates generally to CMOS (complementary metal-oxide-semiconductor) devices and processes and more specifically to such devices and a process for

their fabrication
wherein the sources and drains of the devices are surrounded by
collars of opposite conductivity type. Conventional CMOS technology
tends to be a high mask count processing sequence due to the
necessity of complementary MOS transistors on the same semiconductor
chip. This article describes a key simplification to the CMOS
process sequence which will result in lower processing costs.
Complementary MOS transistors are implemented by using appropriately
doped collars surrounding the MOS source and drain in a fashion
similar to a DMOS device been1|. The nMOS transistor employs a p-doped
collar; the pMOS transistor employs an n-doped collar.
These collars
are formed within a highly resistive (n, f, or i) starting material
through the same oxide opening as the respective sources and drains.
A sample cross-section of two complementary

MOS transistors (such as
would be used to realize an inverter)
fabricated using the p and n
collar technology proposed is shown in the
figure. Two distances are
important in device design (shown on nMOS
only): L, the metallurgical
MOS channel length, and L1, the collar
separation. The MOS threshold
is determined by the collar doping and gate
work function for L1
below a critical value; hence, the choice of L1
can be made, as
appropriate, independent of device thresholds.
The simplified
process sequence consists of polysilicon gate
formation, followed by
the (self-aligned) deposition, in turn, of collar
and source/drain
doping species through a common mask
opening.
Lateral diffusion of
the collars under the gate determines L1 .
Latch-up susceptibility of
the proposed CMOS technology would be at
least as low as a
conventional bulk CMOS process, and most

probably lower due to the
presence of the highly resistive starting material. This occurs for
the following reasons: latch-up in general is due to the interaction
between two parasitic bipolar transistors (npn and pnp) configured as
a cross-coupled latch. As shown herein, the high resistivity
material forms a spacer between the base and collector of each
parasitic bipolar device. The result is a npin and pnip cross-coupled
latch. The current gain b of these two bipolar transistors is
reduced due to the presence of the i layer been2-4|; hence, the proposed
technology has a lower latch-up susceptibility.

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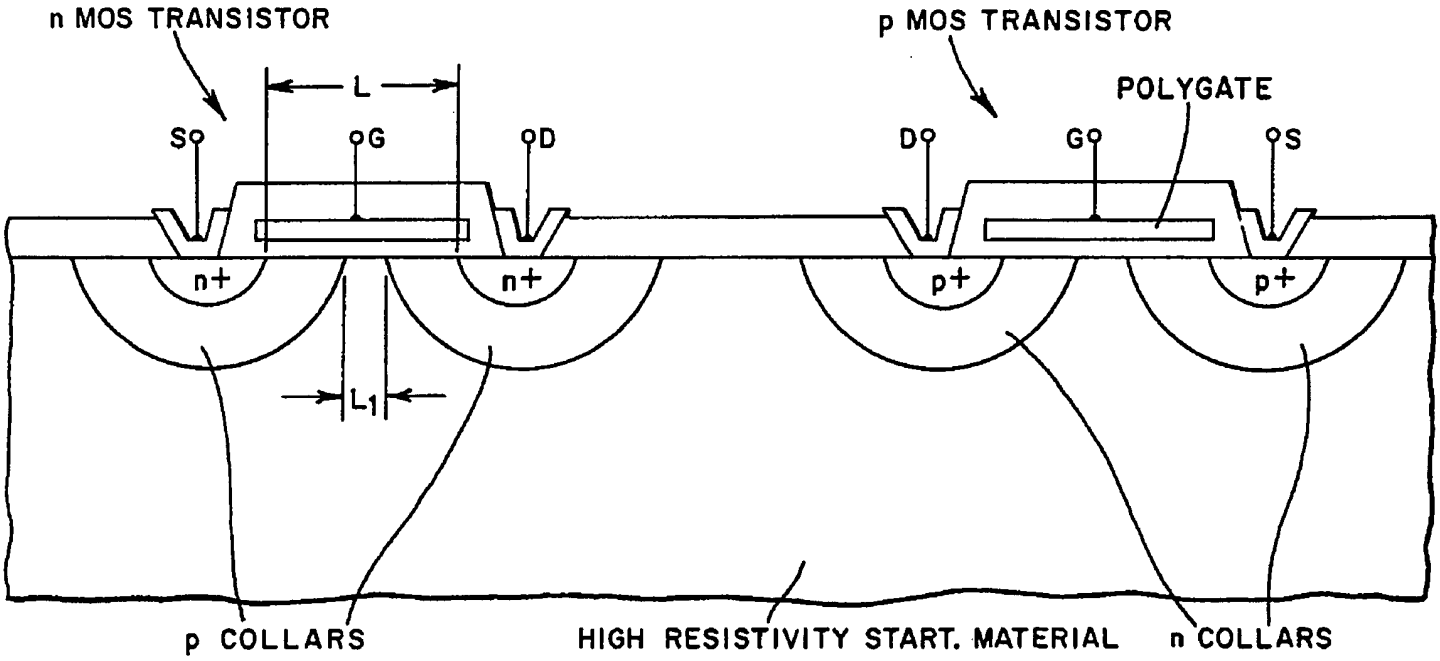
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HIGH RESISTIVITY START. MATERIAL
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DERWENT-ACC-NO: 2002-081637

DERWENT-WEEK: 200211



TITLE: Circuit structure for avoiding latch-up phenomenon - for use in complementary metal oxide semiconductor transistor to prevent the occurrence of latch-up caused by the parasitic bipolar transistor

INVENTOR: SHIA, L

PATENT-ASSIGNEE: UNITED MICROELECTRONICS CORP[UNMIN]

PRIORITY-DATA: 1999TW-0106103 (April 16, 1999)

PATENT-FAMILY:

| PUB-NO | PUB-DATE |
|---|---|

| LANGUAGE | PAGES | MAIN-IPC |
|---|---|---|
| TW 442950 A | June 23, 2001 | |
| N/A | 000 | H01L 027/10 |

APPLICATION-DATA:

| PUB-NO | APPL-DESCRIPTOR |
|---|---|
| APPL-NO | APPL-DATE |
| TW 442950A | N/A |
| 1999TW-0106103 | April 16, 1999 |

INT-CL (IPC): H01L027/10

ABSTRACTED-PUB-NO: TW 442950A

BASIC-ABSTRACT:

NOVELTY - This invention is about circuit structure for avoiding latch-up phenomenon. The N-type contact point is located inside the N-type doped region. The P-type metal oxide semiconductor (MOS) transistor is located inside the N-type doped region, in which the gate of P-type MOS transistor is connected with the input terminal; the source of P-type MOS transistor is

connected with both voltage source and the first N-type MOS transistor. For
the first N-type MOS transistor, the gate is connected with the input terminal;
the source is connected with the ground terminal; and the drain is connected
with drain as well as the output terminal of P-type MOS transistor, and the
second N-type of MOS transistor. For the second N-type of MOS transistor, the
gate is connected with the output terminal, the source is connected with
voltage source, and the drain is connected with the N-type contact point.

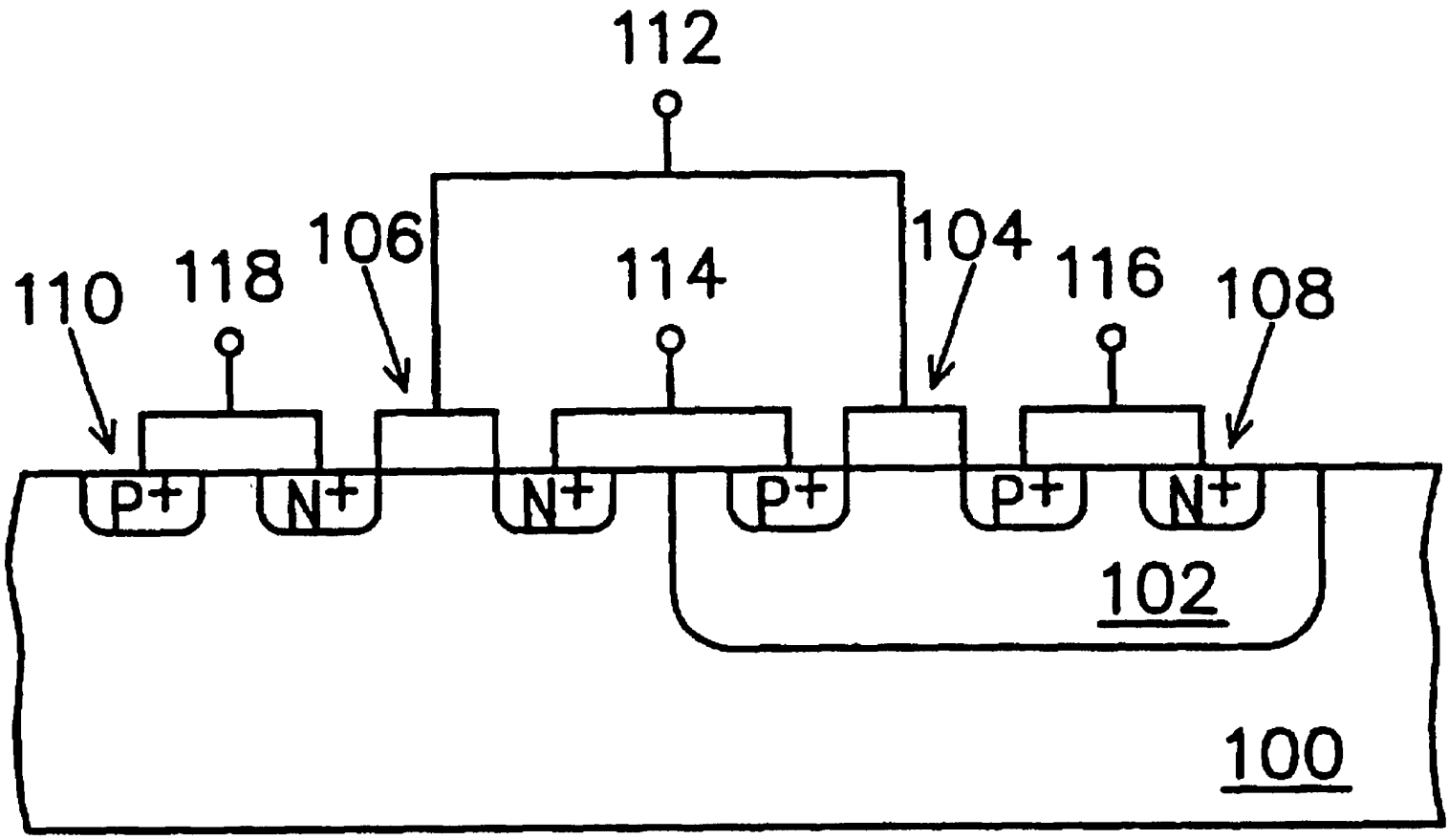
CHOSEN-DRAWING: Dwg.1/1

TITLE-TERMS: CIRCUIT STRUCTURE AVOID LATCH UP PHENOMENON
COMPLEMENTARY METAL
OXIDE SEMICONDUCTOR
TRANSISTOR PREVENT OCCUR LATCH UP CAUSE
PARASITIC BIPOLAR TRANSISTOR

DERWENT-CLASS: U13

EPI-CODES: U13-D02A;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers:
N2002-060722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